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06ES33

Third Semester B.E. Degree Examination, June-July 2009
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Express the P. O. S. equations in a Maxterms list (decimal notations) form. **(04 Marks)**

i) $T = f(a, b, c) = (a + \bar{b} + c)(a + \bar{b} + c)(\bar{a} + \bar{b} + c)$

ii) $J = f(A,B,C,D) = (A+\bar{B}+C+D)(A+\bar{B}+C+\bar{D})(\bar{A}+B+C+D)(\bar{A}+\bar{B}+C+D)(\bar{A}+B+\bar{C}+D)(\bar{A}+\bar{B}+\bar{C}+D)$

b. Reduce the following function using K-map technique and implement using gates. **(10 Marks)**

i) $f(P, Q, R, S) = \Sigma m (0, 1, 4, 8, 9, 10) + d(2, 11)$

ii) $f(A, B, C, D) = \pi M (0, 2, 4, 10, 11, 14, 15)$

c. Design a logic circuit with inputs P, Q, R so that output S is high whenever P is zero or whenever Q = R = 1. **(06 Marks)**

2 a. Using Quine Mccluskey Method and simply the following function.

$f(a, b, c, d) = \Sigma m (0, 1, 2, 3, 8, 9)$ **(10 Marks)**

b. Write the Map entered variable K-map for the Boolean function.

$f(w, x, y, z) = \Sigma m (2, 9, 10, 11, 13, 14, 15)$ **(10 Marks)**

3 a. Implement following multiple output function using 74LS138 and extend gates.

$F_1(A, B, C) = \Sigma m (1, 4, 5, 7)$

$F_2(A, B, C) = \pi M (2, 3, 6, 7)$ **(06 Marks)**

b. Implement full subtractor using decoder and write a truth table. **(08 Marks)**

c. Write a note on encoders. **(06 Marks)**

4 a. Design 2-bit comparator using gates. **(12 Marks)**

b. Implement the following Boolean function using 8 : 1 multiplexer.

$F(A, B, C, D) = \bar{A}B\bar{D} + ACD + \bar{B}CD + \bar{A}\bar{C}D$ **(08 Marks)**

PART – B

5 a. Clearly distinguish between

i) Synchronous and asynchronous circuits.

ii) Combinational and sequential circuits **(06 Marks)**

b. Explain the operation of clocked SR flip-flop. **(08 Marks)**

c. What is race around condition? Discuss in detail. **(06 Marks)**

6 a. Draw the logic diagrams for (i) SR latch (ii) Master – slave JK flip-flop (iii) Master-slave SR flip-flop. **(06 Marks)**

b. Explain the working of 4-bit asynchronous counter. **(06 Marks)**

c. Explain Johnson counter with its circuit diagram and timing diagram. **(08 Marks)**

7 a. Explain with suitable logic and timing diagram.

i) Serial-in serial-out shift register.

ii) Parallel-in parallel-out shift register. **(10 Marks)**

b. Explain the Meoly model and Moore model for clocked synchronous sequential network. **(10 Marks)**

8 a. Compare Moore and Meelay models. **(04 Marks)**

b. Design a synchronous counter using JK flip-flops to count in the sequence 0,1,2,4,5,6,0,1,2..... Use state diagram and state table. **(12 Marks)**

c. State the rules for state assignments. **(04 Marks)**

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